LARGE-SIGNAL DESIGN OF MMIC HIGH EFFICIENT POWER AMPLIFIER

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ABSTRACT

A large-signal two-stage power amplifier design approach using the Waveform-Balance method is presented. The MMIC amplifier designed by this technique is shown here to have a state-of-the-art power and efficiency performances at X-band. The amplifier has 40 percent bandwidth, 2 to 3 watt CW output power, 10 dB power gain, and greater than 30 percent power-added efficiency across most of the frequency band.

INTRODUCTION

The development of a broadband high efficiency MMIC power amplifier presents a great challenge to the young GaAs MMIC technology. To achieve the performance goal, good MESFET device characteristics, such as high breakdown voltage, high current, and high transconductance are the necessary requirements. However, having only the good device characteristics is not sufficient. The matching circuits of the amplifier need to be carefully designed by large-signal method to fully utilize the power and efficiency capability of the MESFET device. In this work, we present a nonlinear amplifier design method, which utilize an accurate nonlinear MESFET model, and the Waveform-Balance simulation program. A two-stage MMIC X-band power amplifier was designed by this technique. Measurement data shows that this large-signal designed amplifier has a state-of-the-art power and efficiency performances for ion-implanted MMIC.

In the large-signal design approach, the nonlinear models of the MESFETs are first developed. These FET models are developed from S-parameter measurements of the MESFETs at various bias voltages (1-3). This nonlinear modeling approach has been shown to be accurate at both small and large signal conditions. A fast nonlinear circuit analysis algorithm called Waveform-Balance method (1-3) was used to simulate the nonlinear model. Using Waveform-Balance, the power contours of the MESFETs were generated and the optimum load impedances were found at the passband frequencies of the amplifier. These computer generated data were used to design the interstage and output-stage matching circuits of the MMIC amplifier.

DESIGN APPROACH

The amplifier is a two-stage design due to the gain requirement. The first stage uses two 1.5 mm x 0.6 μm FETs to drive four 1.8 mm x 0.6 μm FETs at the second stage. The nonlinear models for the 1.5 and 1.8 mm FETs are first developed. In the modeling approach, the S-parameters of the FET is first measured at various bias voltages (2). Small-signal equivalent circuits are then extracted at each bias condition using FET-FITTER (4). Next, the nonlinear elements, G_m, C_{gs}, and R_o versus bias voltages curves are plotted out. Empirical nonlinear expression are then used to fit these curves. Using these nonlinear MESFET models, power contours of the 1.5 and 1.8 mm FETs are generated and the optimum load impedances are found by the Waveform-Balance computer program. The Waveform-Balance method is different from the better known Harmonic-Balance method. In Waveform-Balance, the steady-state solution is sampled and optimized in the time-domain. This method has been shown to have good accuracy and speed.

The contours are simulated at bias condition of VD = 7 V and ID = 1/3 I_{dss}, which is the condition that the class AB amplifier to be operated at. As an example, Figure 1 is the power contours of the 1.5 mm FET at 9 GHz generated by the Waveform-Balance program. From the contours plot, the optimum load impedance presented to the device is found. These contours are generated at 6, 8, 10, and 12 GHz for both the 1.5 and 1.8 mm FETs. The optimum load impedance versus frequency data for the 1.8 and 1.5 mm FETs are plotted in Figures 2 and 3.

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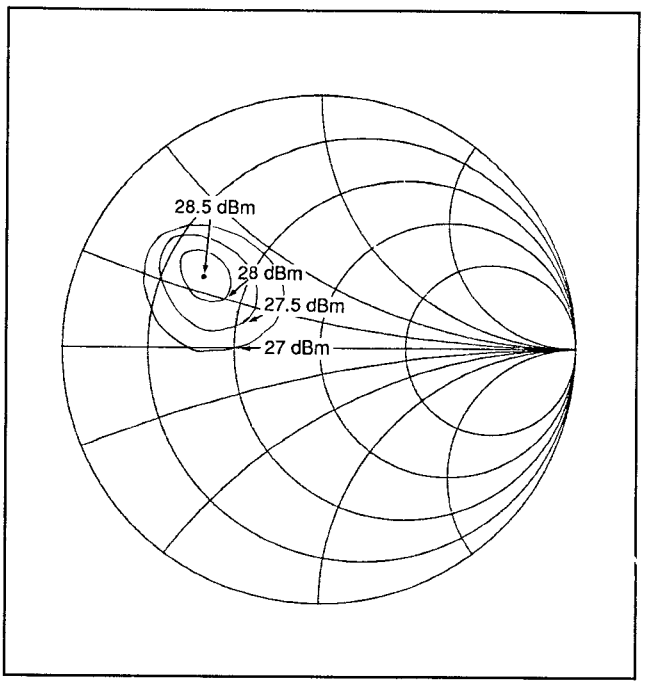

Figure 1 Power contours for the 1.5 mm FET at 9 GHz P_{in} = 22 dBm, Z_{in} = 5+8j, P_{out} = 27 – 28 dBm, 0.5 dB step.

The output matching circuit is first synthesized and then optimized by SuperCompact (5). The optimization goal is to have the output matching circuit presents the optimum load impedances to each one of the 1.8 mm FET at the second stage. The resulting impedances are shown in Figure 2 along with the optimum values. Next, the interstage matching circuit is synthesized and then optimized. The optimization goal is to have the load impedances presented to each 1.5 mm first stage FET match with the optimum values. The resulting impedances are shown in Figure 3 along with the optimum values. By comparing Figure 2 with Figure 3, it can be seen that the interstage matching is more difficult to design for broad-band power-match due to the higher impedance transformation ratio. The final step is the input matching circuit design. The input matching circuit is optimized to give the amplifier high and flat small-signal gain across the frequency band.

SIMULATED AND MEASURED PERFORMANCES

The amplifier power performance is simulated by the Waveform-Balance program. In the amplifier simulation, the S-parameters of the designed input-stage, interstage, and output-stage matching circuits are first generated by SuperCompact. These S-parameter data are then entered into the Waveform-Balance program for the complete amplifier simulation. Figure 4 is the simulated output power versus frequency data for different input power levels.

The amplifier was fabricated by a standard ion-implantation MMIC process (6). The photograph of the fabricated MMIC amplifier is shown in Figure 5. The amplifier was diced and packaged in a test-fixture for power measurement. Figures 6 and 7 are the measured output power and power-added efficiency versus frequency data at the bias condition of VD = 7 V and ID = 1/3 I_{dss}. The amplifier has about 40 percent bandwidth, 2 to 3 watt CW output power, and greater than 30 percent power-added efficiency across most of the frequency band. The agreement between the measured and the simulated data are good except at the low-end of the frequency band.

CONCLUSION

A design method for the two-stage high efficiency power amplifier is presented. The design method utilizes an accurate

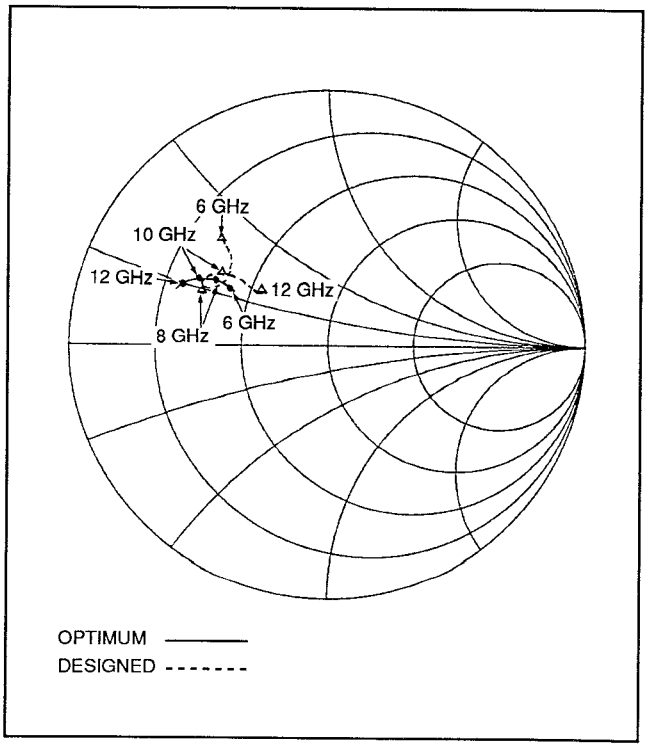

Figure 2 Optimum load impedances and the designed impedances for the 1.8 mm FET.

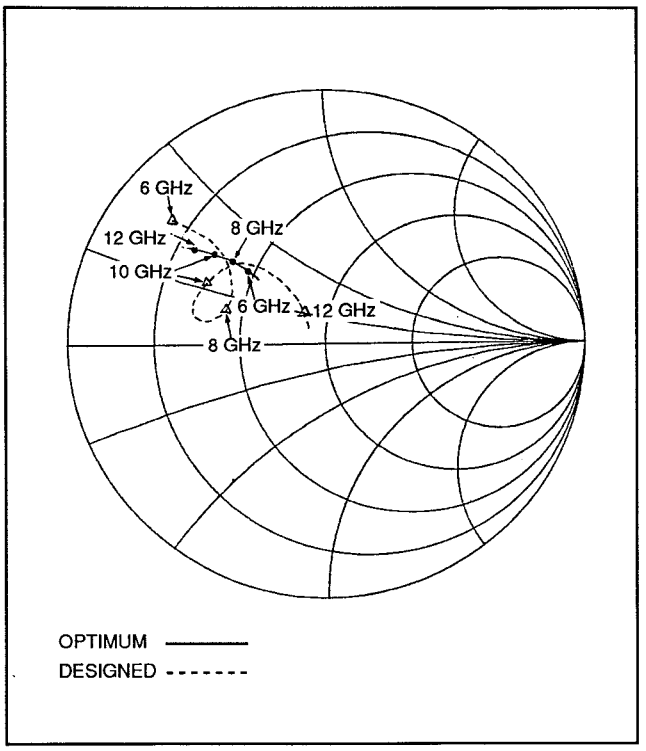

Figure 3 Optimum load impedances and the designed impedances for the 1.5 mm FET.

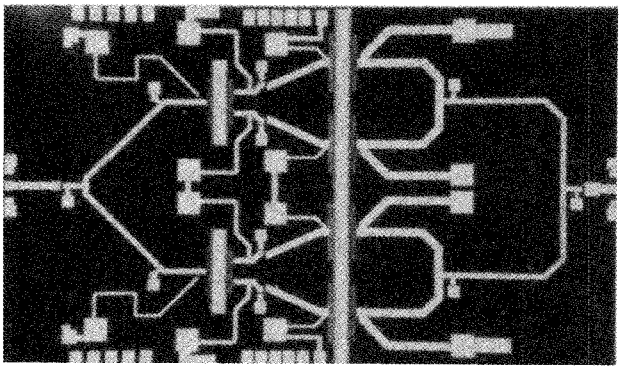

Figure 5 Photo of the MMIC two-stage amplifier.

nonlinear MESFET model, and the Waveform-Balance simulation program. The MMIC amplifier designed by this approach shows excellent power and power-added efficiency.

REFERENCE

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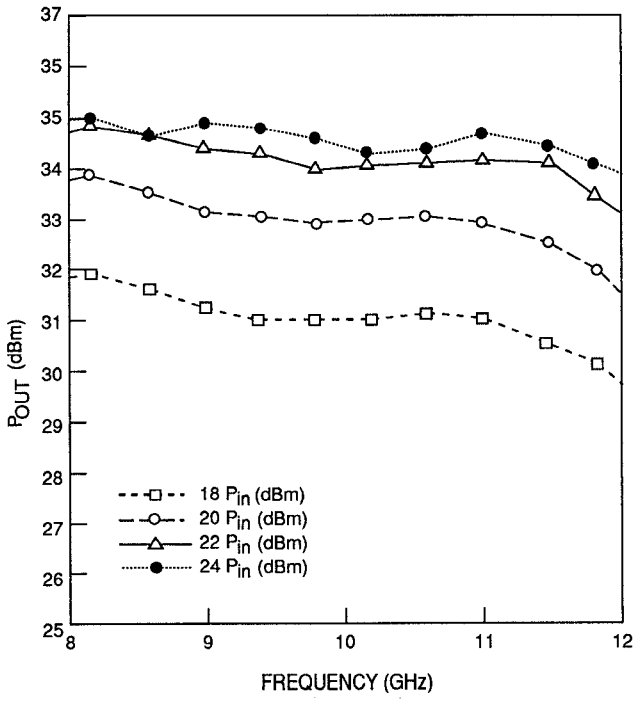

Figure 4 Waveform-Balance simulated output power versus frequency data.

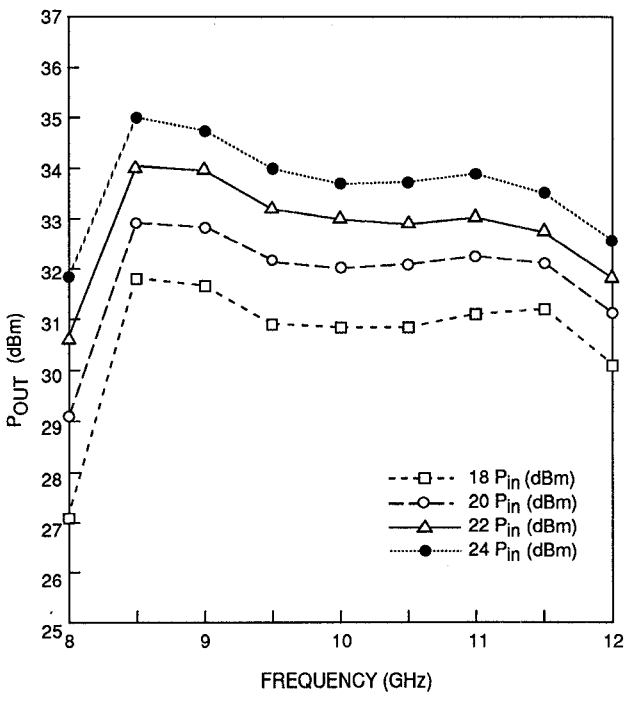

Figure 6 Measured output power versus frequency data.

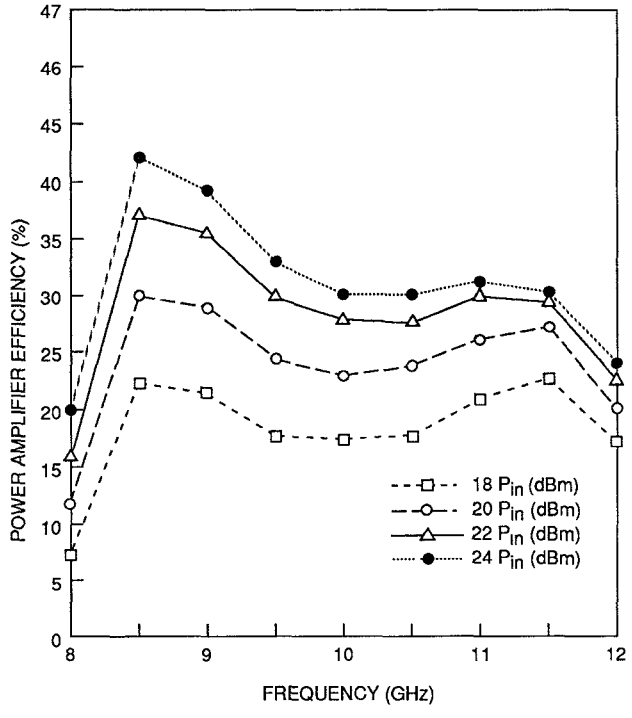

Figure 7 Measured power-added efficiency versus frequency data.

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